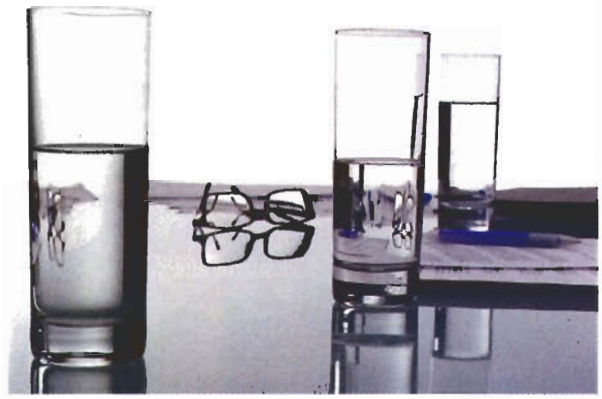

VOICES

Round table mulls hard-IP-at-board-level concept

Sometimes, a panel discussion ends up more like a round table. That scenario happened at DesignCon in February, with a panel that design consultant Pallab Chatterjee organized on hard IP (intellectual property) and whether it can exist for board-level designs. At the chip level, "hard IP" refers to a block of circuitry that a designer has verified, placed, and routed, so that you can drop it into a chip design intact during the physical-design process. In some cases, you can insert hard IP into the design at the foundry just before mask creation.

Can a similar concept exist for board-level design? Chatterjee opened the discussion, observing that some board-level reference designs go all the way to specifying components and providing Gerber files for creating board film. But then he pointed to several examples of designs in which the form factor of the final product makes it impossible to use the reference design without significant modification, and this modification invalidates the electrical verification designers perform on the reference design.

The panelists included Chatterjee; Vipul Badoni, senior manager of the high-speed-I/O-Applications-engineering group at Altera; Jerry Durand, chief executive officer of Durand Interstellar; and John Isaac, director of market development for the systems-design division at Mentor Graphics.

What comes with an Altera reference board?

A Badoni: "If you purchase one of our reference designs, you get a full [Cadence] Allegro database with constraints, schematics, and documentation with design guidelines. We even give you the guidelines we gave to the pc-board designer to design our board.

Isaac: One of the most important things chip vendors deliver to customers are models. Any customer today that takes a reference design as a drop-in core, slaps it in their design, adds a little logic, and intends to make 100 of them is crazy. The performance of signal-integrity models that vendors supply is important.

How much information do you have to model that is in the reference design that may not be just datasheet specs of the FPGA? Do you provide signal-integrity models for the traces that connect the reference design to the outside world?

A Badoni: Yes. We work with vendors to get connection models in with our reference designs. In modeling, if you get garbage in, you get garbage out, so you have to be careful with what you supply. Don't substitute a Micron DIMM for an Infineon DIMM and expect it to work. You have to secure the right models to make sure they work.

What are the worst problems designers face today?

A Badoni: The most prevalent problem we are dealing with today is power delivery.

Durand: It's a problem because of built-in contradictions. For instance, the power-delivery specs on complex chips often say the parts are supposed to have low impedance to the power and ground planes. But if that chip is in a MicroBGA package, you are using 6-mil laser-drilled vias that go down only 0.005 in., or one layer. So, it gets hard to have super low impedance to power and ground planes that are 0.020 in. below the via.

Badoni: Monitoring the power-delivery systems is also tough because you have to model passives in Spice, which is not inherently a passive-modeling technology. You have to figure out what capacitors you can put in your system.

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Durand: Power is a big problem, especially in MicroBGA packages in which a single device can have a mix of pins with different voltages. Layout is difficult with alternating 2.5, 1.8, and 3.3V pins. You can't even run a heavy bus up to catch those pins. If you had four in a row, you could drill a via to connect them, but if you intersperse them, you wind up with fine traces running your power into the lead; it is the only physical way to do it.

Who owns SIP (system-in-package) design: IC designers, pc-board designers, or a separate group?

A Chatterjee: Speaking from the chip-design world, I don't know anyone who would willingly want to take on that set of problems.

Isaac: One of the advantages of SIPs is that a lot of the parts are off-the-shelf. You may design an IC to put in a SIP and then grab parts from other people and add some discretes. It soon becomes a cross between IC and pc-board design.

–by Ron Wilson and Michael Santarini